

FIG. 1

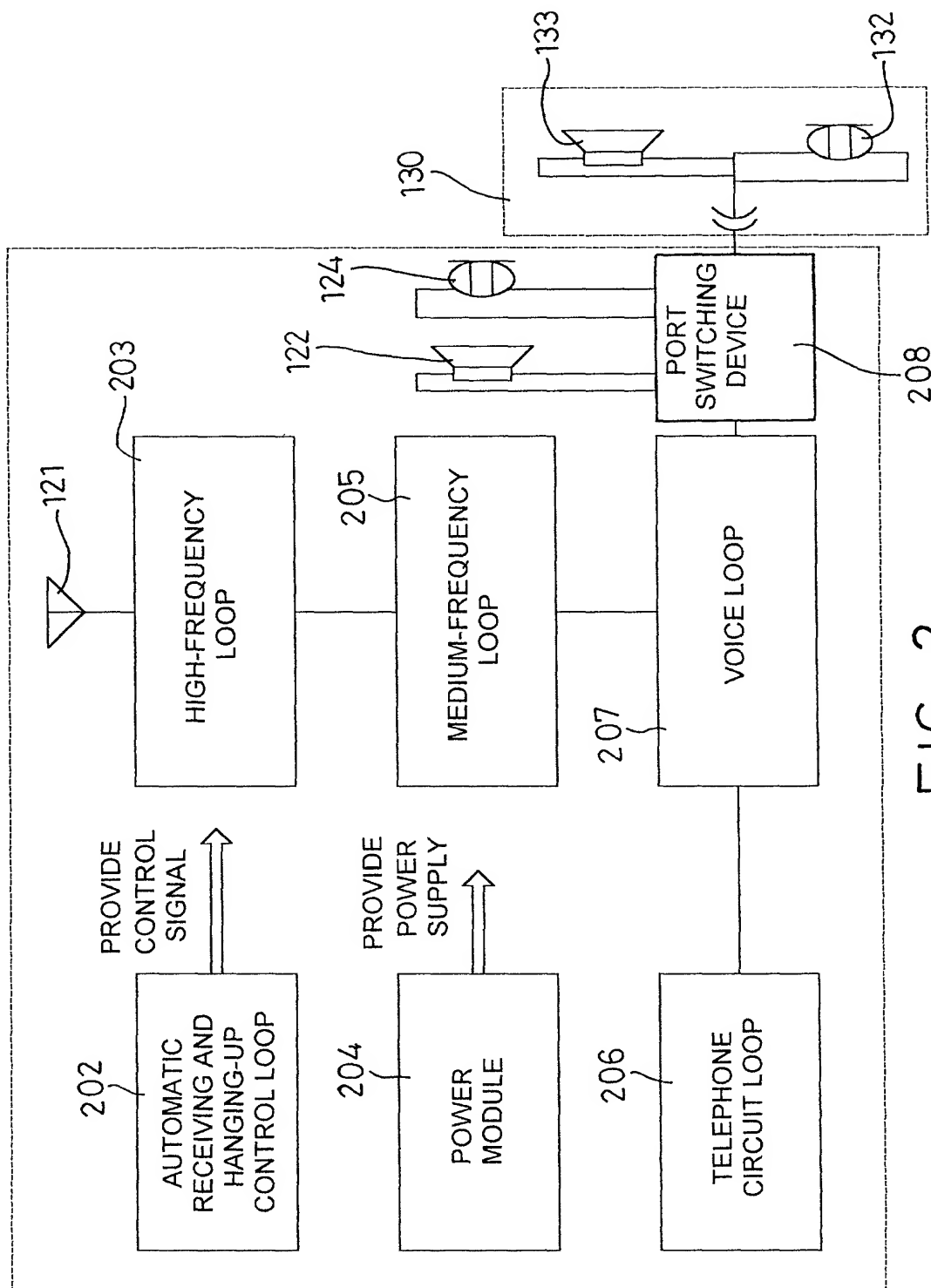


FIG. 2



FIG. 4 is a schematic diagram of the circuit of the present invention, showing the interconnection of the various components.

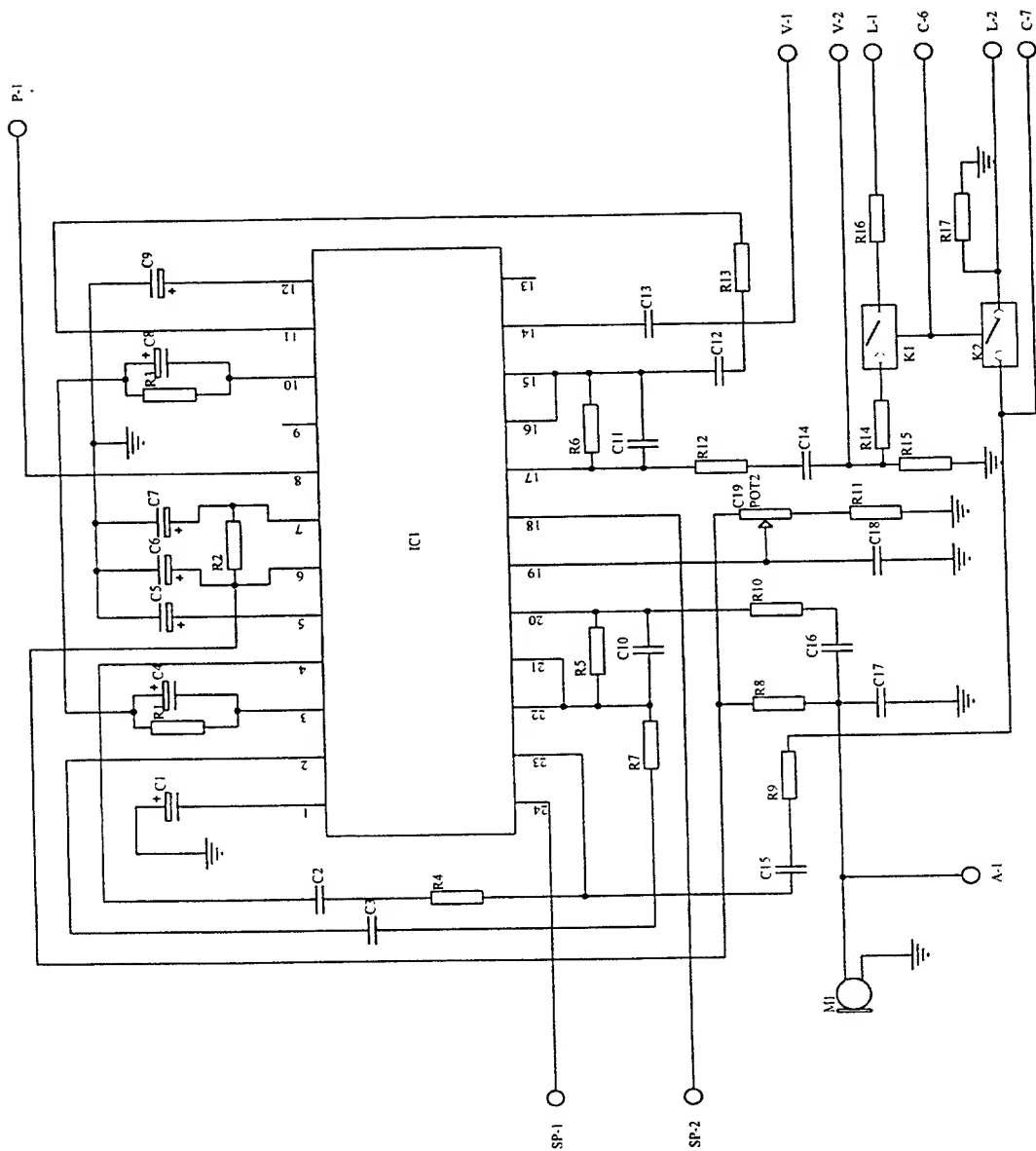


FIG. 4

FIG. 5 is a schematic diagram of a circuit for testing a device under test (DUT) in a test environment. The circuit includes a power source (e.g., a battery) connected to a switch (A-1) and a switch (SP-1). The switch (A-1) is connected to a node (A) and a node (B). The switch (SP-1) is connected to a node (C) and a node (D). The node (A) is connected to the DUT. The node (B) is connected to the DUT. The node (C) is connected to the DUT. The node (D) is connected to the DUT. The DUT is connected to ground.

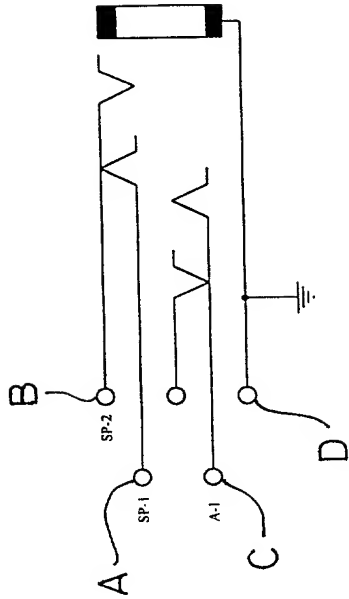


FIG. 5